APS Scientific Computation Seminar Series

Speaker:
Yatish Kumar, ESnet

Title:
EJ-FAT (ESnet JLab - FPGA Accelerated Transport)

Date:
February 12, 2024

Time:
1:00 p.m. (Central Time)

Location:
Join ZoomGov Meeting
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Abstract:
EJ-FAT is an FPGA enhanced switch and load balancer for streaming DAQ data. It is designed to dynamically send event data streams to compute nodes, whilst grouping related DAQ events with nanosecond resolution into common compute nodes for coherent event identification. It solves practical issues for connecting different networking domains at different labs, whilst maintaining a real time processing pipeline at 100s of Gbps. EJ-FAT is a production oriented system that can be deployed locally at APS or tested remotely on the IRI Testbed. It is backed by both ESnet's co-design mandate, as well as the emerging HPDF facility.